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Susumu MATSUMOTO, et al. : Confirmation Number: 4853
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For: ELECTRONIC DEVICE AND METHOD FOR FABRICATING THE SAME

LETTER

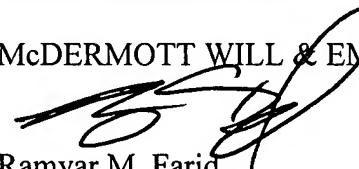
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Sir:

We are submitting for your convenience a duplicate copy of the Certified English Translation of Japanese Patent Application Number 2003-104499 submitted with the fully responsive amendment, filed on August 7, 2007.

Respectfully submitted,

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DECLARATION

I, the undersigned, of #407, Tojiji-cho 26-1, Nakagyo-ku, Kyoto, Japan, hereby certify that I am well acquainted with the English and Japanese languages, that I am an experienced translator for patent matter, and that the attached document is a true English translation of /

Japanese Patent Application No. **2003-104499**

that was filed in Japanese.

I declare that all statements made herein of my own knowledge are true, that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Signature:

A handwritten signature in black ink that appears to read "Tomoko Tanaka".

Tomoko Tanaka

Dated: July 18, 2007

formed over the low dielectric constant film.

[Claim 6] The electronic device of Claim 5, characterized in that the low density insulating film contains nitrogen.

[Claim 7] The electronic device of Claim 5, characterized by further comprising a
5 nitrogen-containing insulating film formed under the low dielectric constant film.

[Claim 8] The electronic device of Claim 1, 3 or 5, characterized in that the low dielectric constant film is a carbon-containing silicon oxide film or a porous film.

[Claim 9] The electronic device of Claim 8, characterized in that the carbon-containing silicon oxide film is a SiOC film.

10 [Claim 10] A method for fabricating an electronic device, characterized by comprising:

the step of forming a nitrogen-non-containing insulating film and a low dielectric constant film in sequence over a nitrogen-containing insulating film;

the step of forming a hole in the low dielectric constant film;

15 the step of applying a chemically amplified resist on the low dielectric constant film with the hole formed therein, and subjecting the chemically amplified resist to exposure and development processes, thereby forming a resist film having an opening in a predetermined region that includes a region in which the hole is formed; and

20 the step of etching the low dielectric constant film with the resist film used as a mask, thereby forming a trench which is connected with the hole.

[Claim 11] The method of Claim 10, characterized in that the hole-forming step includes the step of forming the hole in the low dielectric constant film and the nitrogen-non-containing insulating film, and

25 the method further includes, after the trench-forming step, the step of removing part of the nitrogen-containing insulating film which is located under the hole.

[Claim 12] A method for fabricating an electronic device, characterized by comprising:

the step of forming a nitrogen-non-containing insulating film and a nitrogen-containing insulating film in sequence over a low dielectric constant film;

5 the step of forming a hole in the low dielectric constant film with the nitrogen-non-containing insulating film and the nitrogen-containing insulating film formed thereon;

the step of applying a chemically amplified resist over the low dielectric constant film with the hole formed therein, and subjecting the chemically amplified resist to exposure and development processes, thereby forming a resist film having an opening in a
10 predetermined region that includes a region in which the hole is formed; and

the step of etching the low dielectric constant film with the resist film used as a mask, thereby forming a trench which is connected with the hole.

[Claim 13] The method of Claim 10 or 12, characterized in that the nitrogen-non-containing insulating film is deposited by a CVD process.

15 [Claim 14] The method of Claim 10 or 12, characterized by further comprising, between the hole-forming step and the resist-film forming step, the step of forming a dummy plug in the hole.

[Claim 15] A method for fabricating an electronic device, characterized by comprising:

20 the step of forming a low density insulating film whose film density is 1.3 g/cm^3 or lower on a low dielectric constant film;

the step of forming a hole in the low dielectric constant film with the low density insulating film formed thereon;

25 the step of applying a chemically amplified resist over the low dielectric constant film with the hole formed therein, and subjecting the chemically amplified resist to

exposure and development processes, thereby forming a resist film having an opening in a predetermined region that includes a region in which the hole is formed; and

the step of etching the low dielectric constant film with the resist film used as a mask, thereby forming a trench which is connected with the hole.

5 [Claim 16] The method of Claim 15, characterized by further comprising, after the low-density-insulating-film forming step, the step of subjecting the low density insulating film to a heat treatment or applying light to the low density insulating film.

[Claim 17] The method of Claim 16, characterized in that the light is an electron beam or ultraviolet radiation.

10 [Claim 18] The method of Claim 10, 12 or 15, characterized in that the low dielectric constant film is a carbon-containing silicon oxide film or a porous film.

[Claim 19] The method of Claim 18, characterized in that the carbon-containing silicon oxide film is a SiOC film.

[Detailed Description of the Invention]

15 [0001]

[Technical Field to which the Invention Belongs]

The present invention relates to electronic devices and methods for fabricating the same, and more particularly relates to techniques for forming interconnects.

[0002]

20 [Prior Art]

As the number of devices integrated on a single integrated circuit has been increasing these days, spaces between interconnects have become narrower, causing electric parasitic capacitance occurring between those interconnects to be increased. On the other hand, the line-to-line electric parasitic capacitance has to be reduced in the integrated circuit, which is required to operate at higher speed.

[0003]

In order to lower the line-to-line electric parasitic capacitance, methods for reducing the relative dielectric constant of an insulating film provided between the interconnects have been considered. Proposed as a technique that provides the largest
5 reduction in the line-to-line electric parasitic capacitance is, for example, to use, as the insulating film between the interconnects, a film (i.e., a low dielectric constant film) made of material whose dielectric constant is lower than that of a silicon oxide film. The examples of the low dielectric constant film include a carbon-containing silicon oxide film and a porous film, for example. Carbon-containing silicon oxide films contain carbon in
10 the form of a bulky alkyl or phenyl group. The density (which is from about 1.0 to about 1.3 g/cm³) of a carbon-containing silicon oxide film is thus lower than the density (which is about 2.3 g/cm³) of a silicon oxide film, and the relative dielectric constant (which is from about 2.0 to about 3.0) of the carbon-containing silicon oxide film is also lower than the relative dielectric constant (which is from about 3.9 to about 4.3) of the silicon oxide
15 film.

[0004]

Since the film density of a low dielectric constant film, such as a carbon-containing silicon oxide film, is lower than that of a conventional insulating film, e.g., a silicon oxide film, provided between interconnects, the low dielectric constant film, when exposed to the
20 air, is likely to absorb nitrogen or the like present in the air. Consequently, when a photolithography process for forming a trench pattern for upper-level metal interconnects is performed on the carbon-containing silicon oxide film with a via hole formed therein, for example, the following problem occurs. The photoresist applied cannot be developed sufficiently where it is located near the via hole, which causes the unnecessary photoresist
25 around the via hole to remain. The desired trench pattern thus cannot be formed. This

problem occurs for the following reasons. An amine present in the carbon-containing silicon oxide film with the via hole formed therein, or a basic material or the like derived from nitrogen present in a silicon carbon nitride film formed under the carbon-containing silicon oxide film diffuses through the via hole into the photoresist (which is a chemically amplified resist) on the carbon-containing silicon oxide film. As a result, the base concentration in the resist increases to neutralize an acid generated from an acid-generating material in the resist when the resist is exposed to light applied for the trench pattern formation. This prevents continuous acid-generating reaction from proceeding in the resist, which is an acrylic-based resist, for example, resulting in the insufficient development. This phenomenon is called resist poisoning. In the case of resist poisoning, lower-level and upper-level metal interconnects, e.g., are not properly connected to each other, that is, an interconnection failure occurs.

[0005]

To address this problem, a non-patent related document 1 disclosed an interconnection structure for preventing resist poisoning and a method for fabricating the interconnection structure.

[0006]

FIG. 7 is a cross sectional view illustrating the interconnection structure in a conventional electronic device, disclosed in the non-patent related document 1.

[0007]

As shown in FIG. 7, lower-level metal interconnects **2** are formed in a first insulating film **1** formed on a silicon substrate (not shown). Each lower-level metal interconnect **2** is formed of a barrier metal film **2a** and a copper film **2b**, and the first insulating film **1** is formed of a silicon oxide film. On the lower-level metal interconnects **2** and the first insulating film **1**, a second insulating film **3** made of a silicon carbide film is

formed. On the second insulating film 3, a third insulating film 4 made of a carbon-containing silicon oxide film is formed. On the third insulating film 4, a fourth insulating film 5 made of a silicon carbide film is formed. On the fourth insulating film 5, a fifth insulating film 6 made of a carbon-containing silicon oxide film is formed. A via hole 7, 5 which reaches at least one of the lower-level metal interconnects 2, is formed in the second and third insulating films 3 and 4, while a trench for wiring 8, which reaches the via hole 7, is formed in the fourth and fifth insulating films 5 and 6. In the via hole 7 and the trench 8, a barrier metal film 9 and a copper film 10 are formed in sequence to form a via plug 11 and upper-level metal interconnects 12. The via plug 11 connects the lower-level metal 10 interconnects 2 and the upper-level metal interconnects 12.

[0008]

FIGS. 8(a) through 8(f) are cross sectional views indicating process steps of a method for fabricating the conventional electronic device disclosed in the non-patent related document 1, that is, a method for fabricating the electronic device shown in FIG. 7.

15 [0009]

First, as shown in FIG. 8(a), a first insulating film 1 is formed on a silicon substrate (not shown), after which lower-level metal interconnects 2, formed of a barrier metal film 2a and a copper film 2b, are buried in the first insulating film 1.

[0010]

20 Next, as shown in FIG. 8(b), a second insulating film 3 made of a silicon carbide film, a third insulating film 4 made of a carbon-containing silicon oxide film, a fourth insulating film 5 made of a silicon carbide film, a fifth insulating film 6 made of a carbon-containing silicon oxide film, and a sixth insulating film 13 made of a silicon carbide film are deposited in sequence over the first insulating film 1 and the lower-level metal 25 interconnects 2.

[0011]

Then, a photoresist is applied onto the sixth insulating film 13 and a photolithography process is performed on the photoresist, thereby forming a resist film (not shown) having a hole pattern. Thereafter, with the resist film used as a mask, the sixth 5 insulating film 13 and the fifth insulating film 6 are sequentially dry-etched, and then the photoresist is removed by ashing. By these steps, a hole 14, which corresponds to a via hole 7 (see FIG. 8(e)), is formed in the sixth insulating film 13 and the fifth insulating film 6, as shown in FIG. 8(c).

[0012]

10 Subsequently, a photoresist is applied onto the sixth insulating film 13 and a photolithography process is performed on the photoresist, thereby forming a resist film 15 having a desired trench pattern. More specifically, the resist film 15, having openings 15a that correspond to a trench for wiring 8 (see FIG. 8(e)), is formed.

[0013]

15 Next, the sixth insulating film 13, the fifth insulating film 6, the fourth insulating film 5, and the third insulating film 4 are dry-etched in sequence with the resist film 15 having the trench pattern and the sixth and fifth insulating films 13 and 6 having the hole pattern used as masks. By these steps, as shown in FIG. 8(e), the via hole 7 is formed in the third insulating film 4, while the trench 8 is formed in the fourth and fifth insulating 20 films 5 and 6. It should be noted that after the dry-etching process, the resist film 15 is removed and a cleaning process is performed. Thereafter, part (i.e., the via hole 7 formation region) of the second insulating film 3, part (i.e., the trench 8 formation region) of the fourth insulating film 5, and the sixth insulating film 13, each of which is made of a silicon carbide film, are removed at the same time by performing an etchback process on 25 the entire surface of the substrate. By these steps, as shown in FIG. 8(e), the desired via

hole 7 and the desired trench 8 are formed.

[0014]

Next, a barrier metal film 9 and a copper film 10 are deposited in this order on the fifth insulating film 6 so that the via hole 7 and the trench 8 are filled completely.

5 Thereafter, the barrier metal film 9 and the copper film 10 are removed by a CMP (chemical mechanical polishing) process where they are located externally of the trench 8. By these steps, as shown in FIG. 8(f), a via plug 11 is formed in the via hole 7, while upper-level metal interconnects 12 are formed in the trench 8.

[0015]

10 In the non-patent related document 1, it is reported that resist poisoning caused by diffusion of an amine or the like through the hole 14 is suppressed by using the silicon carbide films that contain no nitrogen, as the second, fourth and sixth insulating films 3, 5 and 13.

[0016]

15 [Non-patent related document 1]

M. Fayolle et al., "Proceedings of the 2002 International Interconnect Technology Conference", pp. 39-41

[0017]

[Problems that the Invention is to solve]

20 Nevertheless, in the aforementioned conventional interconnection structure, the fact that the nitrogen-non-containing silicon carbide films, which are poorer in film quality than silicon carbon nitride films, are used instead of using silicon carbon nitride films for the purpose of preventing resist poisoning causes a problem in that the amount of leakage current is increased. In addition, the film stability of the silicon carbide films is poor, 25 which produces another problem in that the film quality varies with passage of time if the

films are left standing after deposited.

[0018]

In view of the above problems, it is therefore an object of the present invention to prevent occurrence of resist poisoning, while suppressing leakage current increase and film 5 quality change with time in insulating films provided between interconnects.

[0019]

[Means for Solving the problems]

In order to achieve the above object, a first inventive electronic device includes: a low dielectric constant film having a hole, a nitrogen-non-containing insulating film 10 formed under the low dielectric constant film, and a nitrogen-containing insulating film formed under the nitrogen-non-containing insulating film.

[0020] In the first inventive electronic device, the nitrogen-non-containing insulating film is interposed between the low dielectric constant film, serving as an insulating film between interconnects, and the underlying nitrogen-containing insulating 15 film. In other words, the low dielectric constant film and the nitrogen-containing insulating film are not in direct contact with each other, which suppresses the nitrogen from entering the low dielectric constant film. Therefore, when a chemically amplified resist is applied onto the low dielectric constant film with the hole formed therein, diffusion of an amine or the like from the low dielectric constant film through the hole into 20 the resist, that is, a resist poisoning phenomenon, is prevented. In addition, since the nitrogen-containing insulating film (e.g., a silicon carbon nitride film) with excellent film quality is formed under the low dielectric constant film, it is possible to prevent leakage current increase or film quality change over time.

[0021] Furthermore, in the first inventive electronic device, if the nitrogen-non- 25 containing insulating film is deposited by, e.g., a plasma CVD (chemical vapor deposition)

process, the film quality of the underlying nitrogen-containing insulating film is stabilized, such that nitrogen contained in the nitrogen-containing insulating film is not likely to be liberated. It is thus possible to more reliably suppress the nitrogen from entering the low dielectric constant film.

5 [0022] It should be noted that the term “nitrogen-non-containing insulating film” as used herein means an insulating film in which nitrogen is contained at a concentration less than 1×10^{19} atoms/cm³.

10 [0023] In the first inventive electronic device, a lower surface of the low dielectric constant film is preferably in contact with an upper surface of the nitrogen-non-containing insulating film.

[0024] Then, it is possible to more reliably suppress the nitrogen from entering the low dielectric constant film.

15 [0025] A second inventive electronic device includes: a low dielectric constant film having a hole, a nitrogen-non-containing insulating film formed over the low dielectric constant film, and a nitrogen-containing insulating film formed over the nitrogen-non-containing insulating film.

20 [0026] In the second inventive electronic device, the nitrogen-non-containing insulating film is interposed between the low dielectric constant film, serving as an insulating film between interconnects, and the nitrogen-containing insulating film provided over the low dielectric constant film. In other words, the low dielectric constant film and the nitrogen-containing insulating film are not in direct contact with each other, which suppresses the nitrogen from entering the low dielectric constant film. Therefore, when a chemically amplified resist is applied over the low dielectric constant film with the hole formed therein, diffusion of an amine or the like from the low dielectric constant film 25 through the hole into the resist, that is, a resist poisoning phenomenon, is prevented. In

addition, since the nitrogen-containing insulating film (e.g., a silicon carbon nitride film) with excellent film quality is formed over the low dielectric constant film, it is possible to prevent leakage current increase or film quality change over time.

[0027] Furthermore, in the second inventive electronic device, the nitrogen-containing insulating film is formed over the low dielectric constant film with the nitrogen-non-containing insulating film interposed therebetween, so that after the low dielectric constant film is formed, the low dielectric constant film is not directly exposed to an atmosphere (such as plasma) that contains nitrogen. It is therefore possible to more reliably suppress nitrogen from entering the low dielectric constant film.

10 [0028] In the second inventive electronic device, an upper surface of the low dielectric constant film is preferably in contact with a lower surface of the nitrogen-non-containing insulating film.

[0029] Then, it is possible to more reliably suppress the nitrogen from entering the low dielectric constant film.

15 [0030] A third inventive electronic device includes: a low dielectric constant film having a hole, and a low density insulating film having a film density of 1.3 g/cm³ or lower and formed over the low dielectric constant film.

[0031] In the third inventive electronic device, the low density insulating film is formed over the low dielectric constant film serving as an insulating film between 20 interconnects. Thus, nitrogen taken into the low dielectric constant film and nitrogen present in the low density insulating film itself are externally released easily through the low density insulating film. This prevents an amine or the like from diffusing only into the hole formed in the low dielectric constant film. Accordingly, when a chemically amplified resist is applied over the low dielectric constant film, the amount of an amine or the like 25 present per unit volume of the resist where the resist is located near the hole is reduced

extremely, which results in the prevention of resist poisoning. It should be noted that in the third inventive electronic device, the density of the low density insulating film is preferably 0.4 g/cm³ or higher in consideration of the stability of the film.

[0032] In the third inventive electronic device, the low density insulating film
5 preferably contains nitrogen.

[0033] Then, the low density insulating film has excellent film quality, thereby preventing leakage current increase or film quality change over time.

[0034] The third inventive electronic device preferably further includes a nitrogen-containing insulating film formed under the low dielectric constant film.

10 [0035] Then, the nitrogen-containing insulating film has excellent film quality, so that leakage current increase or film quality change over time is prevented.

[0036] In the first, second, and third inventive electronic devices, the low dielectric constant film is preferably a carbon-containing silicon oxide film or a porous film.

15 [0037] Then, capacitance between the interconnects is reduced reliably. As the carbon-containing silicon oxide film, a SiOC film may be used.

[0038] A first inventive method for fabricating an electronic device includes: the step of forming a nitrogen-non-containing insulating film and a low dielectric constant film in sequence over a nitrogen-containing insulating film; the step of forming a hole in the low dielectric constant film; the step of applying a chemically amplified resist on the low dielectric constant film with the hole formed therein, and subjecting the chemically amplified resist to exposure and development processes, thereby forming a resist film having an opening in a predetermined region that includes a region in which the hole is formed; and the step of etching the low dielectric constant film with the resist film used as a mask, thereby forming a trench which is connected with the hole.

25 [0039] In the first inventive electronic device fabrication method, after the hole is formed

in the low dielectric constant film, which is formed over the nitrogen-containing insulating film with the nitrogen-non-containing insulating film interposed therebetween, the chemically amplified resist is applied on the low dielectric constant film. In other words, the nitrogen-non-containing insulating film is interposed between the low dielectric constant film and the nitrogen-containing insulating film, such that the low dielectric constant film and the nitrogen-containing insulating film are not in direct contact with each other. This suppresses the nitrogen from entering the low dielectric constant film. Therefore, when the chemically amplified resist is applied onto the low dielectric constant film with the hole formed therein, diffusion of an amine or the like through the hole into the resist, that is, a resist poisoning phenomenon, is prevented. In addition, since the nitrogen-containing insulating film (e.g., a silicon carbon nitride film) with excellent film quality is formed under the low dielectric constant film, it is possible to prevent leakage current increase or film quality change over time.

[0040] Furthermore, according to the first inventive method, if the nitrogen-non-containing insulating film is deposited by, e.g., a plasma CVD process, the film quality of the underlying nitrogen-containing insulating film is stabilized, such that the nitrogen contained in the nitrogen-containing insulating film is not likely to be liberated. As a result, it is possible to more reliably suppress the nitrogen from entering the low dielectric constant film.

[0041] In the first inventive method, the hole-forming step preferably includes the step of forming the hole in the low dielectric constant film and the nitrogen-non-containing insulating film, and the method preferably further includes, after the trench-forming step, the step of removing part of the nitrogen-containing insulating film which is located under the hole.

[0042] Then, it is possible to prevent etching damage and ashing damage to the

interconnects, devices and the like formed under the hole (examples of the etching and ashing damage include, e.g., oxidation of the surfaces of the interconnects, devices and the like).

- [0043] A second inventive method for fabricating an electronic device includes:
- 5 the step of forming a nitrogen-non-containing insulating film and a nitrogen-containing insulating film in sequence over a low dielectric constant film; the step of forming a hole in the low dielectric constant film with the nitrogen-non-containing insulating film and the nitrogen-containing insulating film formed thereon; the step of applying a chemically amplified resist over the low dielectric constant film with the hole formed therein, and
 - 10 subjecting the chemically amplified resist to exposure and development processes, thereby forming a resist film having an opening in a predetermined region that includes a region in which the hole is formed; and the step of etching the low dielectric constant film with the resist film used as a mask, thereby forming a trench which is connected with the hole.

- [0044] According to the second inventive method, after the nitrogen-non-containing insulating film and the nitrogen-containing insulating film are formed in this order over the low dielectric constant film, the hole is formed in the low dielectric constant film. Thereafter, the chemically amplified resist is applied over the low dielectric constant film. In other words, the nitrogen-non-containing insulating film is interposed between the low dielectric constant film and the nitrogen-containing insulating film, so that the low dielectric constant film and the nitrogen-containing insulating film are not in direct contact with each other. This suppresses the nitrogen from entering the low dielectric constant film. Therefore, when the chemically amplified resist is applied over the low dielectric constant film with the hole formed therein, diffusion of an amine or the like through the hole into the resist, that is, a resist poisoning phenomenon, is prevented. In addition, since 20 the nitrogen-containing insulating film (e.g., a silicon carbon nitride film) with excellent

film quality is formed over the low dielectric constant film, it is possible to prevent leakage current increase or film quality change over time.

[0045] Furthermore, according to the second inventive method, since the nitrogen-containing insulating film is formed over the low dielectric constant film with the nitrogen-
5 non-containing insulating film interposed therebetween, the low dielectric constant film is not directly exposed to an atmosphere (such as plasma) that contains nitrogen, after the low dielectric constant film is formed. It is thus possible to more reliably suppress nitrogen from entering the low dielectric constant film.

[0046] In the first and second inventive methods, the nitrogen-non-containing
10 insulating films are preferably deposited by a CVD process.

[0047] Then, if silicon oxide films are formed as the nitrogen-non-containing insulating films by a plasma CVD process in which TEOS, for example, is used, the density (which is about 2.3 g/cm^3) of the silicon oxide films is greater than the density of the low dielectric constant film, which is a carbon-containing silicon oxide film, for
15 example. Thus, the nitrogen-non-containing insulating films formed out of the silicon oxide films function as barrier layers against nitrogen. It is therefore possible to more reliably suppress nitrogen from entering the low dielectric constant film.

[0048] The first and second inventive methods preferably further include, between the hole-forming step and the resist-film forming step, the step of forming a dummy plug
20 in the hole.

[0049] Then, the dummy plug, made of, e.g., an organic material, covers the wall surface of the hole which includes the interface(s) between the low dielectric constant film and the nitrogen-non-containing insulating film(s). More specifically, since the interface(s) and a damage layer in the wall surface of the hole are covered by the dummy
25 plug, nitrogen diffusion from the interface(s) or the damage layer into the hole is

suppressed, thereby reliably avoiding resist poisoning.

[0050] A third inventive method for fabricating an electronic device includes: the step of forming a low density insulating film whose film density is 1.3 g/cm³ or lower on a low dielectric constant film; the step of forming a hole in the low dielectric constant film
5 with the low density insulating film formed thereon; the step of applying a chemically amplified resist over the low dielectric constant film with the hole formed therein, and subjecting the chemically amplified resist to exposure and development processes, thereby forming a resist film having an opening in a predetermined region that includes a region in which the hole is formed; and the step of etching the low dielectric constant film with the
10 resist film used as a mask, thereby forming a trench which is connected with the hole.

[0051] According to the third inventive method, after the low density insulating film is formed on the low dielectric constant film, the hole is formed in the low dielectric constant film. Thereafter, the chemically amplified resist is applied over the low dielectric constant film. Thus, nitrogen taken into the low dielectric constant film and nitrogen present in the low density insulating film itself are externally released easily through the low density insulating film. This prevents an amine or the like from diffusing only into the hole formed in the low dielectric constant film. Accordingly, when the chemically amplified resist is applied over the low dielectric constant film, the amount of an amine or the like present per unit volume of the resist where the resist is located near the hole is
15 reduced extremely, which results in the prevention of resist poisoning. It should be noted that, in the third inventive method, the density of the low density insulating film is
20 preferably 0.4 g/cm³ or higher in consideration of the stability of the film.

[0052] The third inventive method preferably further includes, after the low-density-insulating-film forming step, the step of subjecting the low density insulating film
25 to a heat treatment or applying light to the low density insulating film.

[0053] Then, the film quality of the low density insulating film is stabilized, while a greater amount of nitrogen is released externally from the low dielectric constant film and the low density insulating film through the low density insulating film. In this method, if the light is an electron beam or ultraviolet radiation, the above-mentioned effect is
5 achieved reliably.

[0054] In the first, second, and third inventive methods, the low dielectric constant film is preferably a carbon-containing silicon oxide film or a porous film.

[0055] Then, capacitance between the interconnects is lowered reliably. As the carbon-containing silicon oxide film, a SiOC film may be used.

10 [0056]

[Embodiments of the Invention]

(EMBODIMENT 1)

Hereinafter, an electronic device and a method for fabricating the device in accordance with a first embodiment of the present invention will be described with
15 reference to the accompanying drawings.

[0057]

FIG. 1 is a cross sectional view illustrating an interconnection structure in the electronic device in accordance with the first embodiment.

[0058]

20 As shown in FIG. 1, lower-level metal interconnects **102** are formed in a lower-level insulating film **101** formed on a substrate **100** made of, e.g., silicon. Each lower-level metal interconnect **102** is formed of, e.g., a tantalum-nitride/tantalum multilayer film **102a** and a copper film **102b**. On the lower-level metal interconnects **102** and the lower-level insulating film **101**, a first nitrogen-containing insulating film **103** made of, e.g., a silicon
25 carbon nitride film is formed. On the first nitrogen-containing insulating film **103**, a first

nitrogen-non-containing insulating film **104** made of, e.g., a silicon oxide film is formed. On the first nitrogen-non-containing insulating film **104**, a low dielectric constant film **105** made of, e.g., a carbon-containing silicon oxide film is formed. On the low dielectric constant film **105**, a second nitrogen-non-containing insulating film **106** made of, e.g., a silicon oxide film is formed. On the second nitrogen-non-containing insulating film **106**, a second nitrogen-containing insulating film **107** made of, e.g., a silicon oxynitride film is formed. In the first nitrogen-containing insulating film **103**, the first nitrogen-non-containing insulating film **104** and (the lower portion of) the low dielectric constant film **105**, a via hole **108**, which reaches at least one of the lower-level metal interconnects **102**, is formed. In (the upper portion of) the low dielectric constant film **105**, the second nitrogen-non-containing insulating film **106**, and the second nitrogen-containing insulating film **107**, a trench for wiring **109**, which is connected with the via hole **108**, is formed. In the via hole **108** and the trench **109**, a tantalum-nitride/tantalum multilayer film **110** and a copper film **111** are formed in sequence to form a via plug **112** and upper-level metal interconnects **113**. The via plug **112** connects the lower-level metal interconnects **102** with the upper-level metal interconnects **113**.

[0059]

FIGS. 2(a) through 2(f) are cross sectional views indicating process steps of a method for fabricating the electronic device of the first embodiment, that is, a method for fabricating the electronic device shown in FIG. 1.

[0060]

First, as shown in FIG. 2(a), a lower-level insulating film **101** made of, e.g., a silicon oxide film is formed on a substrate **100** made of, e.g., silicon, after which lower-level metal interconnects **102**, formed of, e.g., a tantalum-nitride/tantalum multilayer film **102a** and a copper film **102b**, are buried in the lower-level insulating film **101**. More

specifically, after the formation of the lower-level insulating film **101**, a resist film (not shown) having a trench pattern for the lower-level metal interconnects is formed on the lower-level insulating film **101** by a photolithography process, and the lower-level insulating film **101** is then dry-etched with the resist film used as a mask, thereby forming 5 a trench for wiring. Thereafter, the tantalum-nitride/tantalum multilayer film **102a** and the copper film **102b** are deposited in this order on the lower-level insulating film **101** so that the trench is filled completely. The multilayer film **102a** and the copper film **102b** are then removed by a CMP process where they are located externally of the trench, thereby forming the lower-level metal interconnects **102**.

10 [0061]

Next, as shown in FIG. 2(a), a first nitrogen-containing insulating film **103** made of, e.g., a silicon carbon nitride film is deposited to a thickness of 50 nm on the lower-level insulating film **101** and the lower-level metal interconnects **102**.

[0062]

15 Subsequently, as shown in FIG. 2(b), a first nitrogen-non-containing insulating film **104** made of, e.g., a silicon oxide film is deposited to a thickness of 50 nm on the first nitrogen-containing insulating film **103**. In this step, the silicon oxide film, serving as the first nitrogen-non-containing insulating film **104**, is deposited by a plasma CVD process in which TEOS, for example, is used. Thereafter, a low dielectric constant film **105** made of, 20 e.g., a carbon-containing silicon oxide film is deposited to a thickness of 450 nm on the first nitrogen-non-containing insulating film **104**. On the low dielectric constant film **105**, a second nitrogen-non-containing insulating film **106** made of, e.g., a silicon oxide film is then deposited to a thickness of 30 nm. In this step, the silicon oxide film, serving as the second nitrogen-non-containing insulating film **106**, is deposited by a plasma CVD process 25 in which TEOS, for example, is used. Thereafter, a second nitrogen-containing insulating

film **107** made of, e.g., a silicon oxynitride film is deposited to a thickness of 50 nm on the second nitrogen-non-containing insulating film **106**. The silicon oxynitride film, serving as the second nitrogen-containing insulating film **107**, will act as an anti-reflection film in a later photolithography process.

5 [0063]

Subsequently, a photoresist is applied onto the second nitrogen-containing insulating film **107** and a photolithography process is performed on the photoresist, thereby forming a resist film (not shown) having a hole pattern. Thereafter, with the resist film used as a mask, the second nitrogen-containing insulating film **107**, the second nitrogen-
10 non-containing insulating film **106**, the low dielectric constant film **105** and the first nitrogen-non-containing insulating film **104** are dry-etched in sequence, and the photoresist is then removed by ashing. By these steps, a via hole **108** is formed, as shown in FIG. 2(c).

[0064]

Next, as shown in FIG. 2(d), a dummy plug **114**, made of, e.g., an organic material,
15 is formed in the via hole **108**. In this embodiment, the dummy plug **114** is formed in such a manner that the upper surface of the dummy plug **114** is higher than the interface between the low dielectric constant film **105** and the second nitrogen-non-containing insulating film **106**. Thereafter, a photoresist is applied onto the second nitrogen-containing insulating film **107** and then a photolithography (exposure and development)
20 process is performed on the photoresist, thereby forming a resist film **115** having a desired trench pattern. More specifically, the resist film **115** having openings **115a** that correspond to a trench for wiring **109** (see FIG. 2(e)) is formed. The regions in which the openings **115a** are formed include the region in which the via hole **108** is formed.

[0065]

25 Next, the second nitrogen-containing insulating film **107**, the second nitrogen-non-

containing insulating film **106** and (the upper portion of) the low dielectric constant film **105** are sequentially dry-etched with the dummy plug **114** and the resist film **115** having the trench pattern used as masks. By this step, the trench **109**, which is connected with the via hole **108**, is formed, as shown in FIG. 2(e). It should be noted that after the dry-etching process, the dummy plug **114** and the resist film **115** are removed and a cleaning process is then performed.

5 [0066]

Subsequently, part of the first nitrogen-containing insulating film **103** formed of the silicon carbon nitride film, which is located under the via hole **108**, is removed by 10 performing an etchback process on the entire surface of the substrate. A tantalum-nitride/tantalum multilayer film **110** and a copper film **111** are then deposited in sequence on the second nitrogen-containing insulating film **107** so that the via hole **108** and the trench **109** are filled completely. The multilayer film **110** and the copper film **111** are then removed by a CMP process where they are located externally of the trench **109**. By these 15 steps, as shown in FIG. 2(f), a via plug **112** is formed in the via hole **108**, while upper-level metal interconnects **113** are formed in the trench **109**. It should be noted that since the second nitrogen-containing insulating film **107** and the second nitrogen-non-containing insulating film **106** do not necessarily have to be left finally, these films may be completely or partially removed by the above-mentioned etchback process or CMP process.

20 [0067]

As described above, in the first embodiment, the first nitrogen-non-containing insulating film **104** is interposed between the low dielectric constant film (i.e., the carbon-containing silicon oxide film) **105** and the first nitrogen-containing insulating film (i.e., the silicon carbon nitride film) **103** located under the low dielectric constant film **105**.
25 Therefore, resist poisoning is suppressed for the following three reasons, despite the fact

that the first nitrogen-containing insulating film **103** is used.

(1) Since the first nitrogen-containing insulating film **103** and the low dielectric constant film **105** are not in direct contact with each other, it is possible to suppress the nitrogen from entering the low dielectric constant film **105**. Therefore, diffusion of an amine or the like through the via hole **108** into the resist, that is, a resist poisoning phenomenon, is prevented in the lithography process for forming the trench **109**.

(2) As the first nitrogen-non-containing insulating film **104**, the silicon oxide film is formed by a plasma CVD process in which TEOS, for example, is used. Thus, the density (which is about 2.3 g/cm³) of the silicon oxide film is greater than the density of the low dielectric constant film **105**, that is, the carbon-containing silicon oxide film. The first nitrogen-non-containing insulating film **104** formed out of the silicon oxide film therefore functions as a barrier layer against the nitrogen, which suppresses the nitrogen from entering the low dielectric constant film **105** more reliably.

(3) Since the first nitrogen-non-containing insulating film **104** is deposited by a plasma CVD process, the film quality of the underlying first nitrogen-containing insulating film **103**, that is, the silicon carbon nitride film, is stabilized. Consequently, the nitrogen contained in the first nitrogen-containing insulating film **103** is not likely to be liberated. More specifically, since the silicon carbon nitride film is exposed to the oxygen-containing plasma, the surface portion of the silicon carbon nitride film undergoes oxidation to have a higher film density. As a result, the surface portion functions as a barrier against diffusion of the nitrogen contained in the silicon carbon nitride film. It is therefore possible to more reliably suppress the nitrogen from entering the low dielectric constant film **105**.

[0068]

In the first embodiment, the effects mentioned above allow resist poisoning to be suppressed, while permitting the formation of the first nitrogen-containing insulating film

103 (e.g., a silicon carbon nitride film) with excellent film quality under the low dielectric constant film **105**. Accordingly, it is possible to prevent leakage current increase or film quality changes with time. Moreover, since the silicon carbon nitride film, serving as the first nitrogen-containing insulating film **103**, does not contain oxygen, the copper films **102b** are not oxidized when the first nitrogen-containing insulating film **103** is deposited on the copper films **102b** that form the lower-level metal interconnects **102**.

[0069]

In addition, in the first embodiment, the second nitrogen-non-containing insulating film **106** is interposed between the low dielectric constant film (i.e., the carbon-containing silicon oxide film) **105** and the second nitrogen-containing insulating film (i.e., the silicon oxynitride film) **107** provided over the low dielectric constant film **105**. Thus, resist poisoning is suppressed for the following three reasons, despite the fact that the second nitrogen-containing insulating film **107** is used.

(1) Since the second nitrogen-containing insulating film **107** and the low dielectric constant film **105** are not in direct contact with each other, it is possible to suppress the nitrogen from entering the low dielectric constant film **105**. Therefore, diffusion of an amine or the like through the via hole **108** into the resist, that is, a resist poisoning phenomenon, is prevented in the lithography process for forming the trench **109**.

(2) As the second nitrogen-non-containing insulating film **106**, the silicon oxide film is formed by a plasma CVD process in which TEOS, for example, is used. Thus, the density (which is about 2.3 g/cm^3) of the silicon oxide film is greater than the density of the low dielectric constant film **105**, that is, the carbon-containing silicon oxide film. Thus, the second nitrogen-non-containing insulating film **106** formed out of the silicon oxide film functions as a barrier layer against the nitrogen, which suppresses the nitrogen from entering the low dielectric constant film **105** more reliably.

(3) Since the second nitrogen-containing insulating film **107** is provided over the low dielectric constant film **105** with the second nitrogen-non-containing insulating film **106** interposed therebetween, the low dielectric constant film **105** is not directly exposed to an nitrogen-containing atmosphere (e.g., plasma) after the low dielectric constant film **105** is formed. It is thus possible to suppress nitrogen from entering the low dielectric constant film **105** more reliably.

[0070]

In the first embodiment, the effects mentioned above allow resist poisoning to be suppressed, while permitting the formation of the second nitrogen-containing insulating film **107** (e.g., a silicon carbon nitride film) with excellent film quality over the low dielectric constant film **105**. Accordingly, it is possible to prevent leakage current increase or film quality changes with time. Moreover, the silicon oxynitride film having the reflection-preventing effect is used as the second nitrogen-containing insulating film **107**. This eliminates the need for forming a new anti-reflection film, made of, e.g., an organic material, in the lithography processes for forming the via hole **108** and the trench **109**, thereby allowing the number of process steps to be reduced. It also becomes easy to ensure the selective ratio of the second nitrogen-containing insulating film **107** with respect to the resist, which makes it easier to etch the second nitrogen-containing insulating film **107**. Furthermore, as described above, no anti-reflection film has to be applied when the trench **109** is formed, such that the upper surface of the dummy plug **114** can be set to the same height as the bottom face of the trench **109** to be formed. This prevents a fence-like residue to remain on the bottom face of the trench **109** in the vicinity of the via hole **108**, when the etching process for forming the trench **109** is performed.

[0071]

Also, in the first embodiment, the first nitrogen-containing insulating film **103** is

left under the via hole **108**, that is, on the lower-level metal interconnects **102**, until the formation of the trench **109** is completed. This reduces damage (e.g., oxidation of the surfaces of the lower-level metal interconnects **102**) to the lower-level metal interconnects **102**, caused by the etching and ashing processes.

5 [0072]

Moreover, in the first embodiment, the dummy plug **114** is formed in the via hole **108** prior to the photolithography process for forming the trench **109**. Therefore, the dummy plug **114** covers the wall surface of the via hole **108**, which includes the interfaces between the low dielectric constant film **105** and the first and second nitrogen-non-containing insulating films **104** and **106**. More specifically, since those interfaces and a damage layer in the wall surface of the via hole **108** are covered by the dummy plug **114**, nitrogen diffusion from the interfaces or the damage layer into the via hole **108** is prevented, thereby reliably avoiding resist poisoning. In addition, the presence of the dummy plug **114** in the via hole **108** allows the surface of the resist applied to be 10 planarized, so that the accuracy of the pattern obtained by the photolithography process is increased.

15 [0073]

In the first embodiment, a silicon oxynitride film having the effect of preventing reflection is used as the second nitrogen-containing insulating film **107**. However, instead 20 of this, another kind of insulating film that contains nitrogen (more accurately, a film containing nitrogen at a concentration of 1×10^{19} atoms/cm³ or higher) may be used. For example, if a silicon nitride film is used as the second nitrogen-containing insulating film **107**, the second nitrogen-containing insulating film **107** can be used as a hard mask in the etching process for forming the via hole **108** or the trench **109**. This is effective in cases 25 where a porous film or a film (i.e., an insulating film having a further lower dielectric

constant) that contains a higher concentration of carbon is used as the low dielectric constant film **105**.

[0074]

In the first embodiment, a silicon carbon nitride film is used as the first nitrogen-containing insulating film **103**. However, instead of this, another kind of insulating film that contains nitrogen may be used.

[0075]

In the first embodiment, silicon oxide films are used as the first and second nitrogen-non-containing insulating films **104** and **106**. Instead of the silicon oxide films, other kinds of insulating films that contain no nitrogen (more accurately, films that contain nitrogen at a concentration less than 1×10^{19} atoms/cm³) may be used.

[0076]

Moreover, in the first embodiment, as the carbon-containing silicon oxide film serving as the low dielectric constant film **105**, a SiOC film, e.g., may be used.

15 [0077]

In the first embodiment, (the lower surface of) the low dielectric constant film **105** is in direct contact with (the upper surface of) the first nitrogen-non-containing insulating film **104**. However, another nitrogen-non-containing insulating film may be provided between the low dielectric constant film **105** and the first nitrogen-non-containing insulating film **104**. Likewise, although (the upper surface of) the low dielectric constant film **105** is in direct contact with (the lower surface of) of the second nitrogen-non-containing insulating film **106**, another nitrogen-non-containing insulating film may be provided between the low dielectric constant film **105** and the second nitrogen-non-containing insulating film **106**.

25 [0078]

Also, although in the first embodiment, the present invention is applied to form the interconnection structure including the lower-level metal interconnects 102 and the upper-level metal interconnects 113 that are connected with each other by the via plug 112, the present invention is not limited to this. It will be obvious that the present invention is applicable to, for example, formation of a memory cell structure including a transistor (i.e., doped layers thereof) and a capacitor (i.e., a lower electrode thereof) that are connected with each other by a contact plug.

[0079]

(Comparative example)

Hereinafter, as a comparative example of the first embodiment, an electronic device having a line-to-line insulating-film structure, in which a low dielectric constant film and a nitrogen-containing insulating film are in direct contact with each other, will be described, and a method for fabricating the device will be also discussed (See pp. 15-17 in "Proceedings of the 2002 International Interconnect Technology Conference" by Kazuyuki Higashi et al.)

[0080]

FIG. 3 is a cross sectional view illustrating the interconnection structure in the electronic device in accordance with the comparative example.

[0081]

As shown in FIG. 3, lower-level metal interconnects 22, made of a tantalum-nitride/tantalum multilayer film 22a and a copper film 22b, are formed in a first insulating film 21 formed on a silicon substrate (not shown). On the lower-level metal interconnects 22 and the first insulating film 21, a second insulating film (a nitrogen-containing insulating film) 23 made of a silicon carbon nitride film is formed. On the second insulating film 23, a third insulating film (a low dielectric constant film) 24 made of a

carbon-containing silicon oxide film is formed. On the third insulating film 24, a fourth insulating film 25 made of a silicon oxide film is formed. The fourth insulating film 25 is formed using plasma which is free of contamination with nitrogen. In the second insulating film 23 and (at least the lower portion of) the third insulating film 24, a via hole 26, which reaches at least one of the lower-level metal interconnects 22, is formed. In (the upper portion of) the third insulating film 24 and the fourth insulating film 25, a trench for wiring 27, which is connected with the via hole 26, is formed. In the via hole 26 and the trench 27, a tantalum-nitride/tantalum multilayer film 28 and a copper film 29 are formed in sequence to form a via plug 30 and upper-level metal interconnects 31. The via plug 30 connects the lower-level metal interconnects 22 with the upper-level metal interconnects 31.

[0082]

FIGS. 4(a) through 4(f) are cross sectional views indicating process steps of a method for fabricating the electronic device according to the comparative example, that is, a method for fabricating the electronic device shown in FIG. 3.

[0083]

First, as shown in FIG. 4(a), a first insulating film 21 is formed on a silicon substrate (not shown), after which lower-level metal interconnects 22, made of a tantalum-nitride/tantalum multilayer film 22a and a copper film 22b, are buried in the first insulating film 21.

[0084]

Next, as shown in FIG. 4(b), a second insulating film 23 made of a silicon carbon nitride film is deposited on the first insulating film 21 and the lower-level metal interconnects 22. Thereafter, the second insulating film 23 is subjected to a plasma treatment so that the film quality of the second insulating film 23 is stabilized.

Subsequently, a third insulating film 24 made of a carbon-containing silicon oxide film is deposited on the second insulating film 23. Then, on the third insulating film 24, a fourth insulating film 25 made of a silicon oxide film is deposited by a plasma CVD process, after which an organic anti-reflection film 32 is formed on the fourth insulating film 25. It
5 should be noted that the fourth insulating film 25 is formed using nitrogen-contamination-free plasma, after the underlying third insulating film 24 is subjected to a pretreatment which is free of nitrogen contamination.

[0085]

Next, a photoresist is applied onto the organic anti-reflection film 32 and a
10 photolithography process is performed on the photoresist, thereby forming a resist film (not shown) having a hole pattern. Thereafter, with the resist film used as a mask, the organic anti-reflection film 32, the fourth insulating film 25 and the third insulating film 24 are sequentially dry-etched, and the photoresist and the organic anti-reflection film 32 are then removed by ashing. By these steps, a via hole 26 is formed, as shown in FIG. 4(c).

15 [0086]

Next, as shown in FIG. 4(d), a lower-level resist film 33 is deposited on the fourth insulating film 25 so that the via hole 26 is filled completely, after which a SOG (spin on glass) film 34 is formed on the lower-level resist film 33. Thereafter, a photoresist is applied onto the SOG film 34 and a photolithography process is performed on the
20 photoresist, thereby forming an upper-level resist film 35 having a desired trench pattern. More specifically, the upper-level resist film 35 having openings 35a that correspond to a trench for wiring 27 (see FIG. 4(e)) is formed.

[0087]

Next, the SOG film 34 is dry-etched with the upper-level resist film 35 having the
25 trench pattern used as a mask. Subsequently, with the patterned SOG film 34 (having the

trench pattern) used as a mask, the lower-level resist film 33, the fourth insulating film 25, and (the upper portion of) the third insulating film 24 are dry-etched in this order. By these steps, as shown in FIG. 4(e), the trench 27, which is connected with the via hole 26, is formed. It should be noted that after the dry-etching process, the upper-level resist film 35, 5 the SOG film 34, and the lower-level resist film 33 are removed and a cleaning process is performed.

[0088]

Next, part of the second insulating film 23 which is located under the via hole 26 is removed by performing an etchback process on the entire surface of the substrate. 10 Thereafter, a tantalum-nitride/tantalum multilayer film 28 and a copper film 29 are deposited in this order on the fourth insulating film 25 so that via hole 26 and the trench 27 are filled completely. The multilayer film 28 and the copper film 29 are then removed by a CMP process where they are located externally of the trench 29. By these steps, as shown 15 in FIG. 4(f), a via plug 30 is formed in the via hole 26, while upper-level metal interconnects 31 are formed in the trench 27.

[0089]

As described above, in the comparative example, the second insulating film 23, that is, the silicon carbon nitride film, is plasma-treated for stabilization of the film quality, thereby suppressing resist poisoning.

20 [0090]

Nevertheless, in the comparative example, nitrogen diffuses from the silicon carbon nitride film (i.e., the second insulating film 23) into the third insulating film (i.e., the low dielectric constant film) 24 that is in direct contact with the silicon carbon nitride film, due to unstable nitrogen remaining within the silicon carbon nitride film or variations in the 25 plasma treatment. As a result, diffusion of an amine or the like by way of the via hole 26

into the resist, that is, a resist poisoning phenomenon, cannot be suppressed sufficiently in the lithography process for forming the trench 27.

[0091]

Also, in the comparative example, after the pretreatment free of nitrogen 5 contamination is performed, the fourth insulating film 25, that is, the silicon oxide film, is formed on the third insulating film (i.e., the low dielectric constant film) 24 by using nitrogen-contamination-free plasma, whereby resist poisoning is suppressed. However, the silicon oxide film has no reflection-preventing effect, such that the organic anti-reflection film 32 has to be provided when the pattern for forming the via hole 26 is formed by 10 lithography. Nevertheless, since the coating film thickness of the organic anti-reflection film 32 is large and it is difficult to secure the selective ratio of the organic anti-reflection film 32 with respect to the photoresist, the etching process for forming the via hole 26 becomes difficult. In addition, as described above, the lower-level resist film 33, the SOG 15 film 34 and the upper-level resist film 35 are used in combination, when the pattern for forming the trench 27 is formed by lithography. This makes it difficult to perform the etching process for forming the trench 27. In this case, if a dimensional deviation or a misalignment occurs in the lithography process, regeneration of the pattern becomes difficult due to the use of the SOG film 34. More specifically, unlike a resist film, the SOG film 34 cannot be removed easily by ashing or the like. In a case where an organic 20 anti-reflection film is formed instead of the combination of the lower-level resist film 33, the SOG film 34 and the upper-level resist film 35, a problem similar to that occurring in the etching process for forming the via hole 26 arises.

[0092]

In cases where a low dielectric constant film having a still lower dielectric constant 25 (specifically, a film whose relative dielectric constant ϵ is lower than 2.8) is used, a

process, in which a nitrogen-containing insulating film such as a silicon nitride film is formed on the low dielectric constant film and then used as a hard mask in an etching process, is effective in terms of achieving a low selective ratio with respect to the photoresist, as well as preventing ashing damage. In the comparative example, however, 5 no structure or process other than that in which a silicon oxide film is formed on a low dielectric constant film without using nitrogen-containing plasma is allowed. In other words, no nitrogen-containing insulating films can be formed on the low dielectric constant film. Thus, considering that the dielectric constant of insulating films will be lowered in the future, the comparative example is disadvantageous. Moreover, in the comparative 10 example, the relative dielectric constant of the above-mentioned silicon oxide film is as high as about 4.2, which causes the problem of increasing capacitance between the interconnects. Therefore, the comparative example is also unfavorable in terms of lowering of dielectric constant required in insulating films in the future.

[0093]

15 In contrast, in the first embodiment, the structure (see FIG. 1), in which the first nitrogen-non-containing insulating film **104** is interposed between the low dielectric constant film **105** and the first nitrogen-containing insulating film **103** located under the low dielectric constant film **105**, and the second nitrogen-non-containing insulating film **106** is interposed between the low dielectric constant film **105** and the second nitrogen-containing insulating film **107** provided over the low dielectric constant film **105**, achieves 20 the outstanding effect of solving all of the above-mentioned problems occurring in the comparative example.

[0094]

(Second embodiment)

25 Hereinafter, an electronic device and a method for fabricating the device in

accordance with a second embodiment of the present invention will be described with reference to the accompanying drawings.

[0095]

FIG. 5 is a cross sectional view illustrating an interconnection structure in the 5 electronic device in accordance with the second embodiment.

[0096]

As shown in FIG. 5, lower-level metal interconnects 202, made of, e.g., a tantalum-nitride/tantalum multilayer film 202a and a copper film 202b, are formed in a lower-level insulating film 201 formed on a substrate 200 made of, e.g., silicon. On the 10 lower-level metal interconnects 202 and the lower-level insulating film 201, a nitrogen-containing insulating film 203 made of, e.g., a silicon carbon nitride film is formed. On the nitrogen-containing insulating film 203, a low dielectric constant film 204 made of, e.g., a carbon-containing silicon oxide film is formed. On the low dielectric constant film 204, a low density insulating film (a low density cap film) 205 whose film density is 1.3 15 g/cm³ or lower is formed. In the nitrogen-containing insulating film 203 and (the lower portion of) the low dielectric constant film 204, a via hole 206, which reaches at least one of the lower-level metal interconnects 202, is formed. In (the upper portion of) the low dielectric constant film 204 and the low density cap film 205, a trench for wiring 207, which is connected with the via hole 206, is formed. In the via hole 206 and the trench 20 207, a tantalum-nitride/tantalum multilayer film 208 and a copper film 209 are formed in sequence to form a via plug 210 and upper-level metal interconnects 211.

[0097]

FIGS. 6(a) through 6(f) are cross sectional views indicating process steps of a method for fabricating the electronic device according to the second embodiment, that is, a 25 method for fabricating the electronic device shown in FIG. 5.

[0098]

First, as shown in FIG. 6(a), a lower-level insulating film 201 made of, e.g., a silicon oxide film is formed on a substrate 200 made of, e.g., silicon, after which lower-level metal interconnects 202, made of, e.g., a tantalum-nitride/tantalum multilayer film 5 202a and a copper film 202b, are buried in the lower-level insulating film 201.

[0099]

Subsequently, as shown in FIG. 6(b), a nitrogen-containing insulating film 203 made of, e.g., a silicon carbon nitride film or a silicon nitride film is deposited to a thickness of 50 nm on the lower-level insulating film 201 and the lower-level metal 10 interconnects 202. Thereafter, a low dielectric constant film 204 made of, e.g., a carbon-containing silicon oxide film is deposited to a thickness of 450 nm on the nitrogen-containing insulating film 203. Subsequently, on the low dielectric constant film 204, a low density cap film 205 whose film density is 1.3 g/cm³ or lower and whose thickness is 50 nm is formed. Thereafter, an organic material, for example, is applied onto the low 15 density cap film 205 to form a first anti-reflection film 212.

[0100]

Next, a photoresist is applied onto the first anti-reflection film 212 and a photolithography process is performed on the photoresist, thereby forming a resist film (not shown) having a hole pattern. Thereafter, with the resist film used as a mask, the first 20 anti-reflection film 212, the low density cap film 205 and the low dielectric constant film 204 are sequentially dry-etched, and the photoresist and the first anti-reflection film 212 are then removed by ashing. By these steps, a via hole 206 is formed, as shown in FIG. 6(c).

[0101]

25 Subsequently, as shown in FIG. 6(d), an organic material, for example, is applied

onto the low density cap film 205 so that the via hole 206 is filled completely, thereby forming a second anti-reflection film 213. Thereafter, a photoresist is applied onto the second anti-reflection film 213, and a photolithography (exposure and development) process is performed on the photoresist, thereby forming a resist film 214 having a desired 5 trench pattern. More specifically, the resist film 214 having openings 214a that correspond to a trench for wiring 207 (see FIG. 6(e)) is formed. The regions in which the openings 214a are formed include the region in which the via hole 206 is formed.

[0102]

Next, with the resist film 214 having the trench pattern used as a mask, the second 10 anti-reflection film 213, the low density cap film 205, and (the upper portion of) the low dielectric constant film 204 are dry-etched in sequence, thereby forming the trench 207, which is connected with the via hole 206, as shown in FIG. 6(e). It should be noted that after the dry-etching process, the remaining second anti-reflection film 213 and the resist film 214 are removed and a cleaning process is performed.

15 [0103]

Subsequently, part of the nitrogen-containing insulating film 203 formed of the silicon carbon nitride film, which is located under the via hole 206, is removed by performing an etchback process on the entire surface of the substrate. Thereafter, a tantalum-nitride/tantalum multilayer film 208 and a copper film 209 are deposited in 20 sequence on the low density cap film 205 so that the via hole 206 and the trench 207 are filled completely. The multilayer film 208 and the copper film 209 are then removed by a CMP process where they are located externally of the trench 207. By these steps, as shown in FIG. 6(f), a via plug 210 is formed in the via hole 206, while upper-level metal interconnects 211 are formed in the trench 207. It should be noted that since the low 25 density cap film 205 does not necessarily have to be left finally, this film may be

completely or partially removed by the above-mentioned etchback process or CMP process.

[0104]

As described above, in the second embodiment, the low density cap film **205** is formed on the low dielectric constant film (i.e., the carbon-containing silicon oxide film) **204**. Thus, nitrogen taken into the low dielectric constant film **204**, nitrogen within the nitrogen-containing insulating film **203**, and nitrogen present in the low density cap film **205** itself are likely to be released externally through the low density cap film **205**. This prevents an amine or the like from diffusing only into the via hole **206** formed in the low dielectric constant film **204**. Accordingly, the amount of the amine or the like present per unit volume of the resist where the resist is located near the via hole **206** is reduced significantly in the lithography process for forming the trench **207**, which results in the prevention of resist poisoning.

[0105]

In the second embodiment, the effects mentioned above allow resist poisoning to be suppressed, while permitting the formation of the nitrogen-containing insulating film **203** (e.g., a silicon carbon nitride film) with excellent film quality under the low dielectric constant film **204**. It is thus possible to prevent leakage current increase or film quality changes with time. Moreover, since the silicon carbon nitride film, serving as the nitrogen-containing insulating film **203**, does not contain oxygen, the copper films **202b** are not oxidized when the nitrogen-containing insulating film **203** is deposited on the copper films **202b** that form the lower-level metal interconnects **202**.

[0106]

Also, in the second embodiment, the nitrogen-containing insulating film **203** is left under the via hole **206**, that is, on the lower-level metal interconnects **202**, until the

formation of the trench **207** is completed. This reduces damage (e.g., oxidation of the surfaces of the lower-level metal interconnects **202**) to the lower-level metal interconnects **202**, caused by the etching and ashing processes.

[0107]

5 Furthermore, in the second embodiment, the second anti-reflection film **213** is buried in the via hole **206**, before the photolithography process for forming the trench **207** is performed. The second anti-reflection film **213** thus covers the wall surface of the via hole **206**. In other words, a damage layer in the wall surface of the via hole **206** is covered by the second anti-reflection film **213**. As a result, nitrogen diffusion from the damage 10 layer into the via hole **206** is suppressed, thereby preventing resist poisoning more reliably.

[0108]

Moreover, in the second embodiment, the kind of insulating film usable as the low density cap film **205** is not limited particularly, so long as the film employed has a film density of 1.3 g/cm^3 or lower. However, if a film that has not only a low density but also a 15 low dielectric constant, for example, a porous film, is used as the low density cap film **205**, capacitance between the interconnects is reduced. More specifically, a porous film, such as a HSQ (hydrogen silsesquioxane) film or a XLK film (whose density is about 0.9 g/cm^3) fabricated by Dow Corning, may be used. If the low density cap film **205** contains nitrogen, the film quality of the low density cap film **205** is improved, so that leakage 20 current increase or film quality changes with time is prevented. On the other hand, it is preferable that the low density cap film **205** does not contain carbon. This is because when a carbon-containing film such as a SiOC film is subjected to an ashing process, carbon is eliminated from the film, causing leakage current to flow easily. It should be noted that the density of the low density cap film **205** is preferably 0.4 g/cm^3 or higher in consideration 25 of the stability of the film.

[0109]

In the second embodiment, in cases where a coating film, for example, a porous film such as the above-mentioned HSQ film, is used as the low density cap film 205, it is preferable that after the formation of the low density cap film 205, the low density cap film 5 205 be subjected to, e.g., a heat treatment at about 300 to 400 C°, or an EB (electron beam) cure process or a DUV (deep ultraviolet) cure process. Then, the quality of the low density cap film 205 is stabilized, while a greater amount of nitrogen is released externally through the low density cap film 205 from the nitrogen-containing insulating film 203, the low dielectric constant film 204, and the low density cap film 205. It should be noted that 10 instead of the EB and the DUV, some other type of light may be applied to the low density cap film 205.

[0110]

Also, in the second embodiment, a carbon-containing silicon oxide film such as a SiOC film, a Silk film, or a porous film such as a MSQ (methyl silsesquioxane) film, for 15 example, may be used as the low dielectric constant film 204.

[0111]

[Effects of the Invention]

In a structure according to the present invention, the nitrogen-containing insulating film is formed under or over the low dielectric constant film with the nitrogen-non-containing insulating film interposed therebetween, so that it is possible to suppress 20 nitrogen from entering the low dielectric constant film. Therefore, when a chemically amplified resist is applied over the low dielectric constant film with the hole formed therein, diffusion of an amine or the like from the low dielectric constant film through the hole into the resist, that is, a resist poisoning phenomenon, can be prevented. In addition, 25 due to the nitrogen-containing insulating film with excellent film quality, it is possible to

prevent leakage current increase or film quality change over time.

[0112]

In another structure according to the present invention, the low density insulating film is formed over the low dielectric constant film. Thus, nitrogen contained in the low
5 dielectric constant film or the like are externally released easily through the low density insulating film. This prevents an amine or the like from diffusing only into the hole formed in the low dielectric constant film. Accordingly, when a chemically amplified resist is applied over the low dielectric constant film, the amount of an amine or the like present per unit volume of the resist where the resist is located near the hole is reduced
10 extremely, which results in the prevention of resist poisoning.

[FIG. 1]

FIG. 1 is a cross sectional view illustrating an interconnection structure in an electronic device in accordance with a first embodiment of the present invention.

[FIG. 2]

15 FIGS. 2(a) through 2(f) are cross sectional views indicating process steps of a method for fabricating the electronic device of the first embodiment of the present invention.

[FIG. 3]

20 FIG. 3 is a cross sectional view illustrating an interconnection structure in an electronic device in accordance with a comparative example.

[FIG. 4]

FIGS. 4(a) through 4(f) are cross sectional views indicating process steps of a method for fabricating the electronic device according to the comparative example.

[FIG. 5]

25 FIG. 5 is a cross sectional view illustrating an interconnection structure in an

electronic device in accordance with a second embodiment of the present invention.

[FIG. 6]

FIGS. 6(a) through 6(f) are cross sectional views indicating process steps of a method for fabricating the electronic device according to the second embodiment of the 5 present invention.

[FIG. 7]

FIG. 7 is a cross sectional view illustrating an interconnection structure in a conventional electronic device.

[FIG. 8]

10 FIGS. 8(a) through 8(f) are cross sectional views indicating process steps of a method for fabricating the conventional electronic device.

[Explanation of the Reference Characters]

- 100 Substrate
- 101 Lower-level insulating film
- 15 102 Lower-level metal interconnect
- 102a Tantalum-nitride/tantalum multilayer film
- 102b Copper film
- 103 First nitrogen-containing insulating film
- 104 First nitrogen-non-containing insulating film
- 20 105 low dielectric constant film
- 106 Second nitrogen-non-containing insulating film
- 107 Second nitrogen-containing insulating film
- 108 Via hole
- 109 Trench
- 25 110 Tantalum-nitride/tantalum multilayer film

- 111 Copper film
- 112 Via plug
- 113 Upper-level metal interconnect
- 114 Dummy plug
- 5 115 Resist film
- 115a Opening
- 200 Substrate
- 201 Lower-level insulating film
- 202 Lower-level metal interconnect
- 10 202a Tantalum-nitride/tantalum multilayer film
- 202b Copper film
- 203 Nitrogen-containing insulating film
- 204 Low dielectric constant film
- 205 Low density cap film
- 15 206 Via hole
- 207 Trench
- 208 Tantalum-nitride/tantalum multilayer film
- 209 Copper film
- 210 Via plug
- 20 211 Upper-level metal interconnect
- 212 First anti-reflection film
- 213 Second anti-reflection film
- 214 Resist film
- 214a Opening

[Name of the Document] Abstract

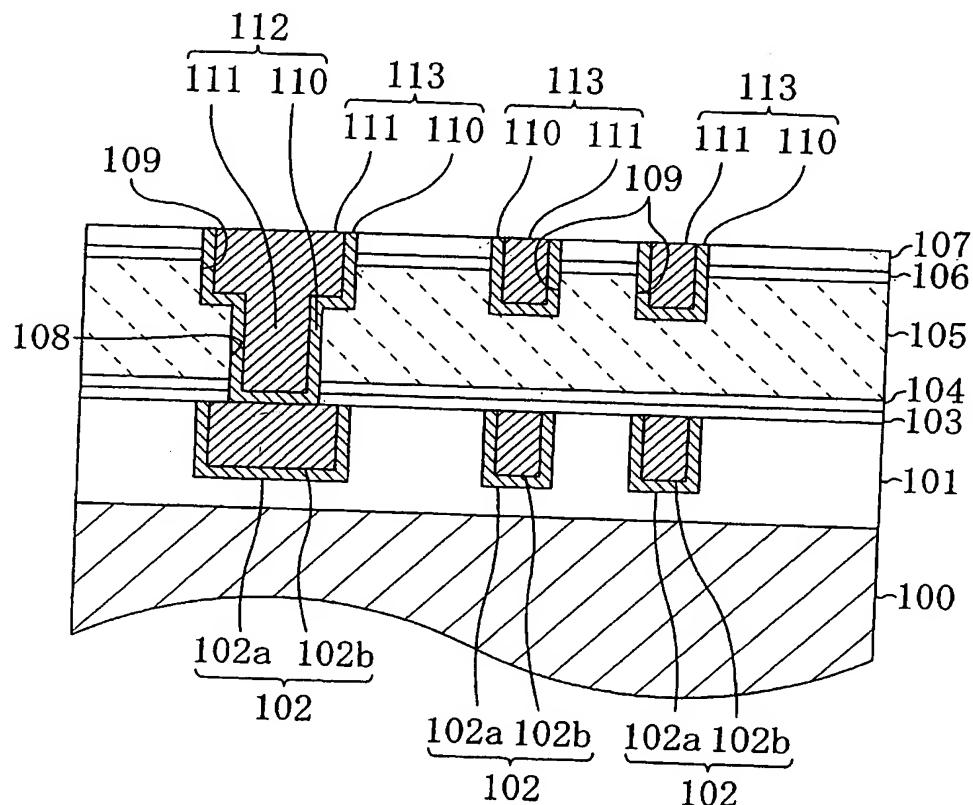
[Abstract]

[Purpose] To protect resist poisoning while preventing leakage current increase or film quality change over time in an insulating film between interconnects.

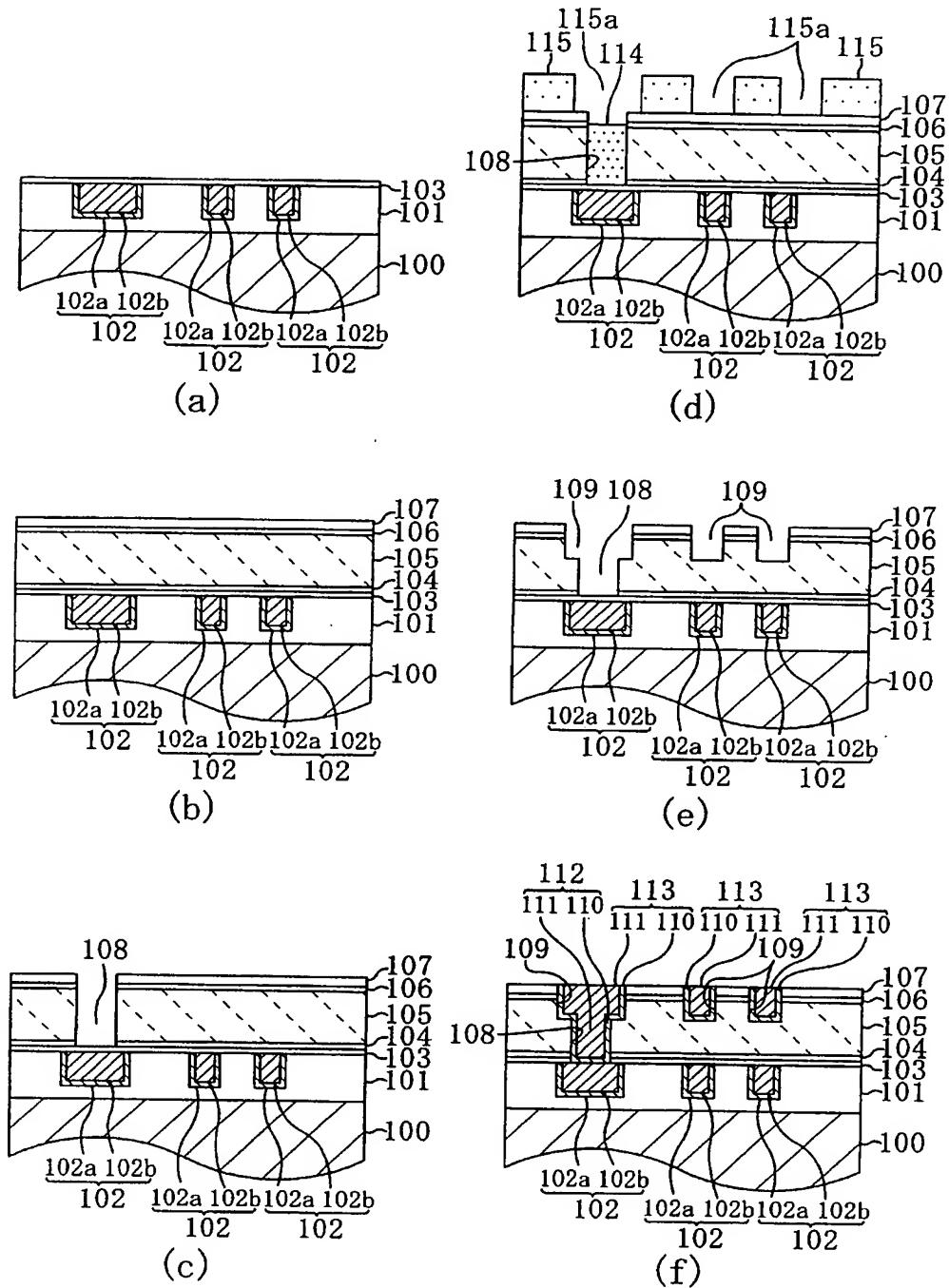
5 [Solution] A first nitrogen-containing insulating film **103** is provided under a low dielectric constant film **105** having a via hole **108** formed therein with a first nitrogen-non-containing insulating film **104** interposed therebetween. Also, a second nitrogen-containing insulating film **107** is formed over the low dielectric constant film **105** with a second nitrogen-non-containing insulating film **106** interposed therebetween.

10 [Selected Figure] FIG. 1

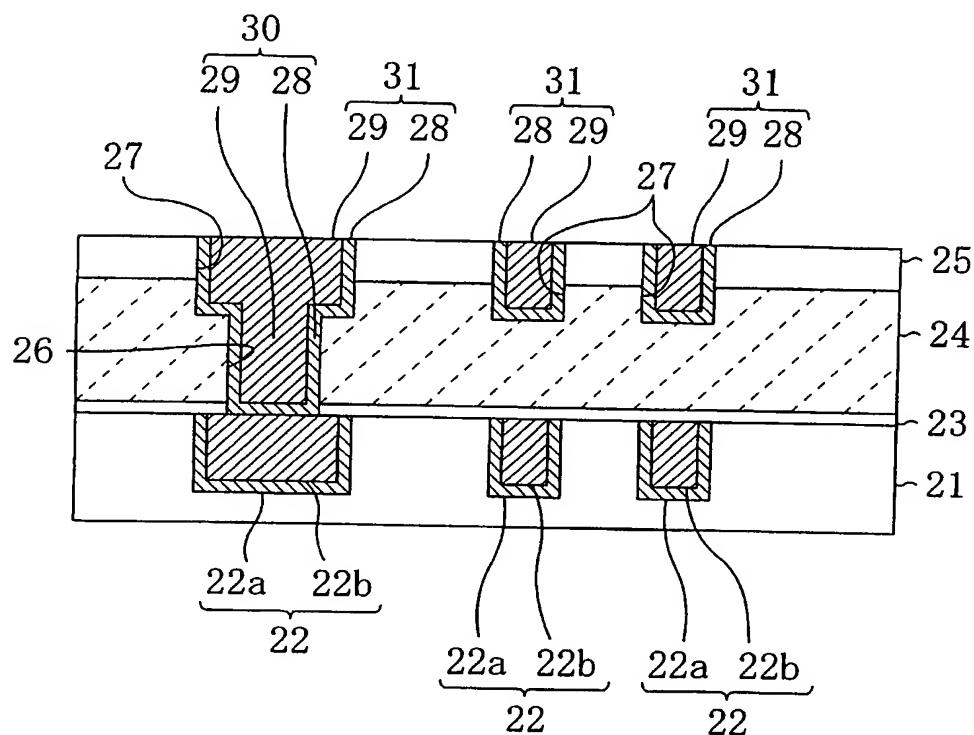
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【図1】 [FIG.1]



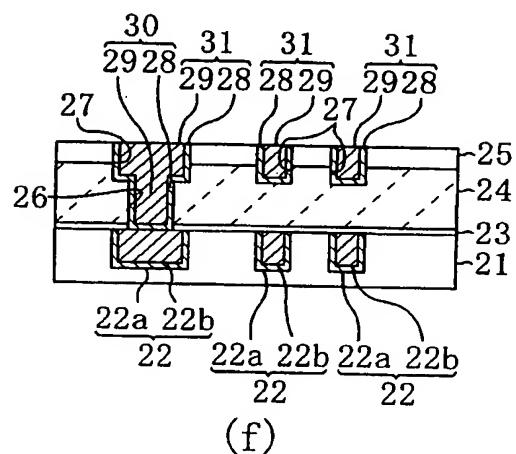
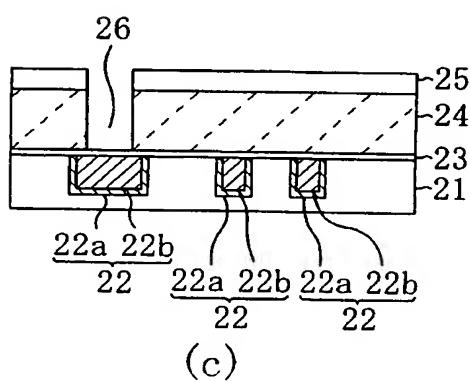
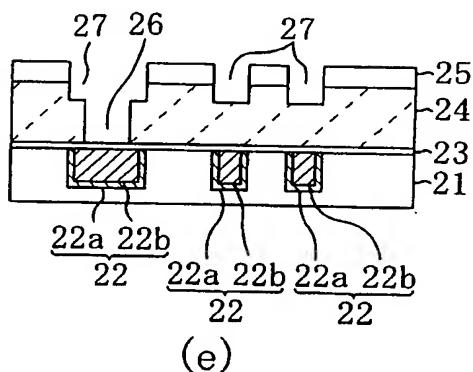
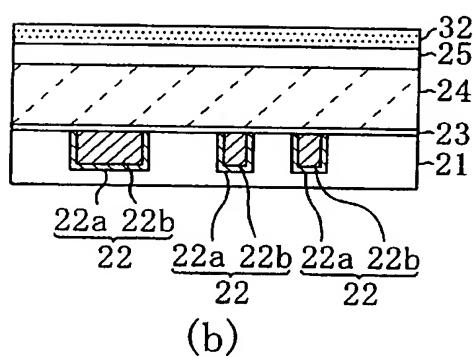
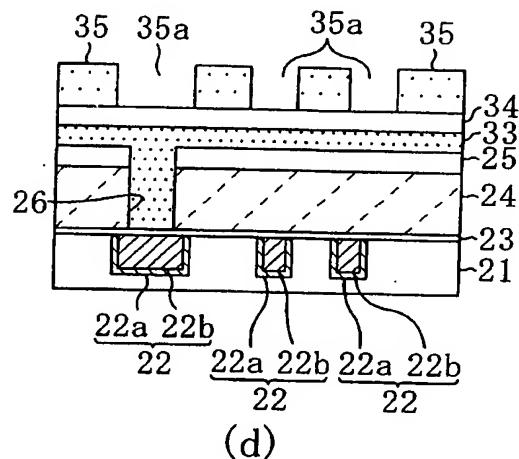
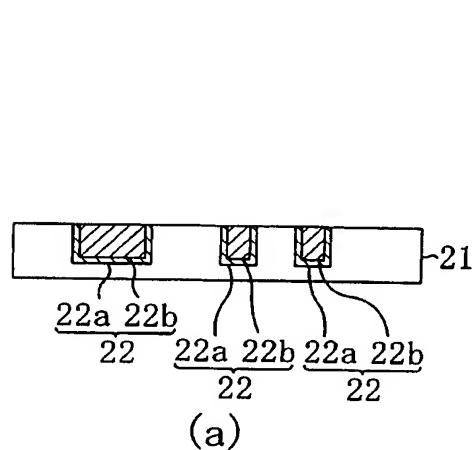
【図2】 [FIG. 2]



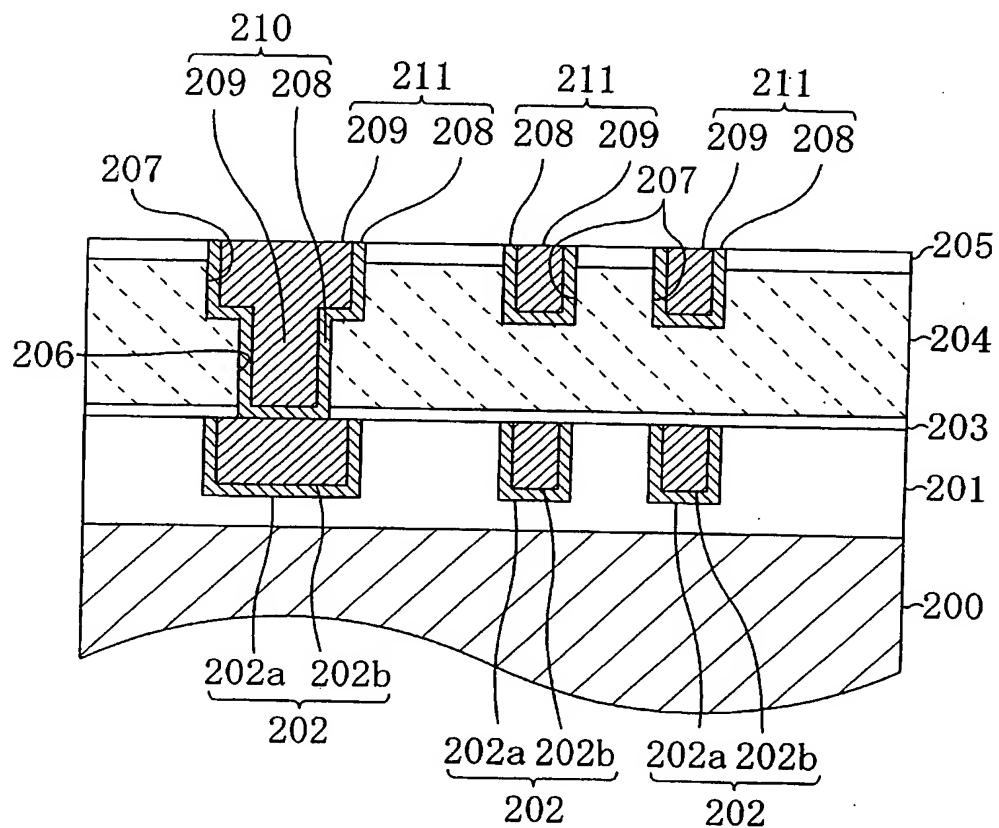
【図3】 [FIG.3]



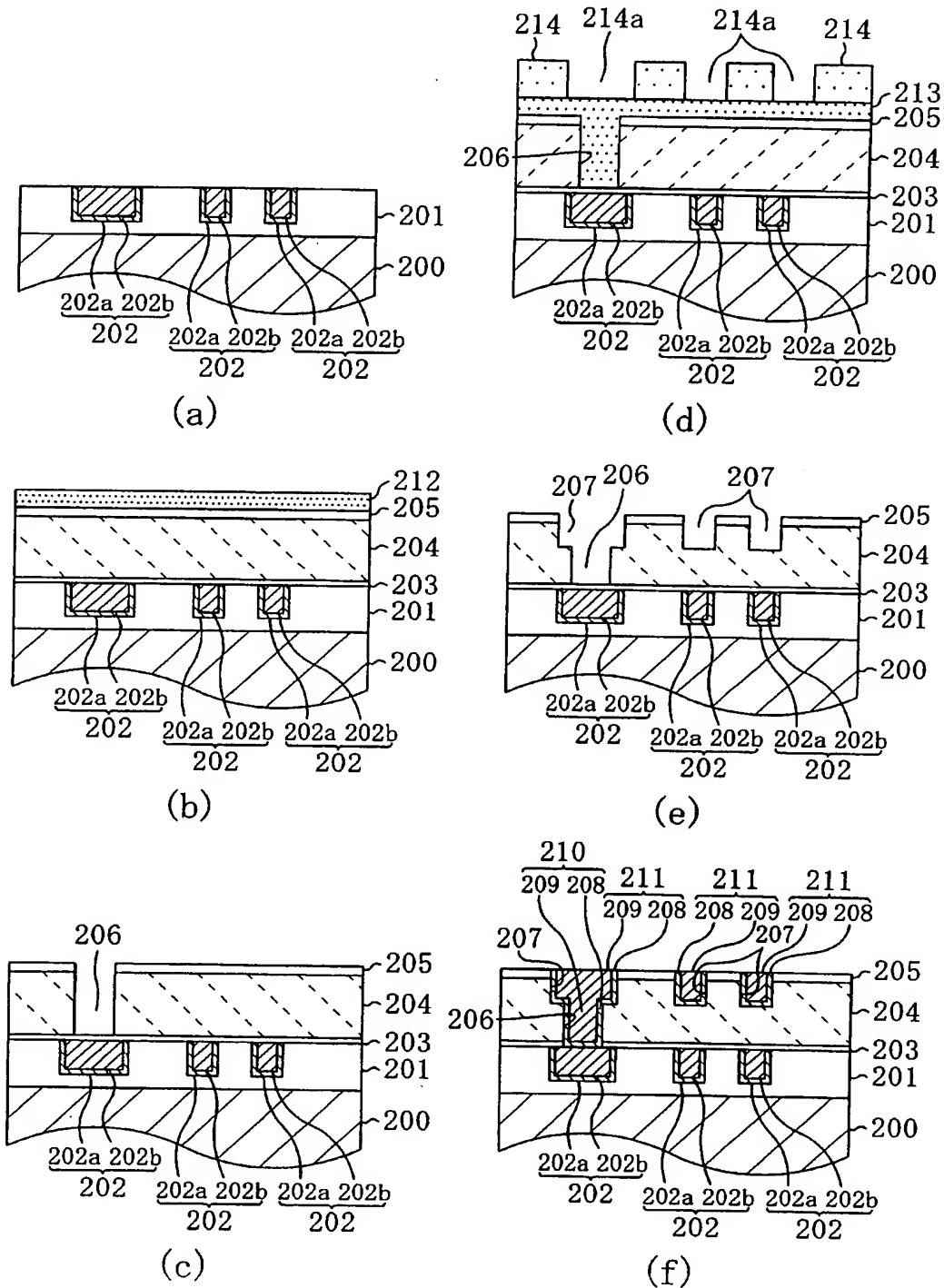
【図4】 [FIG.4]



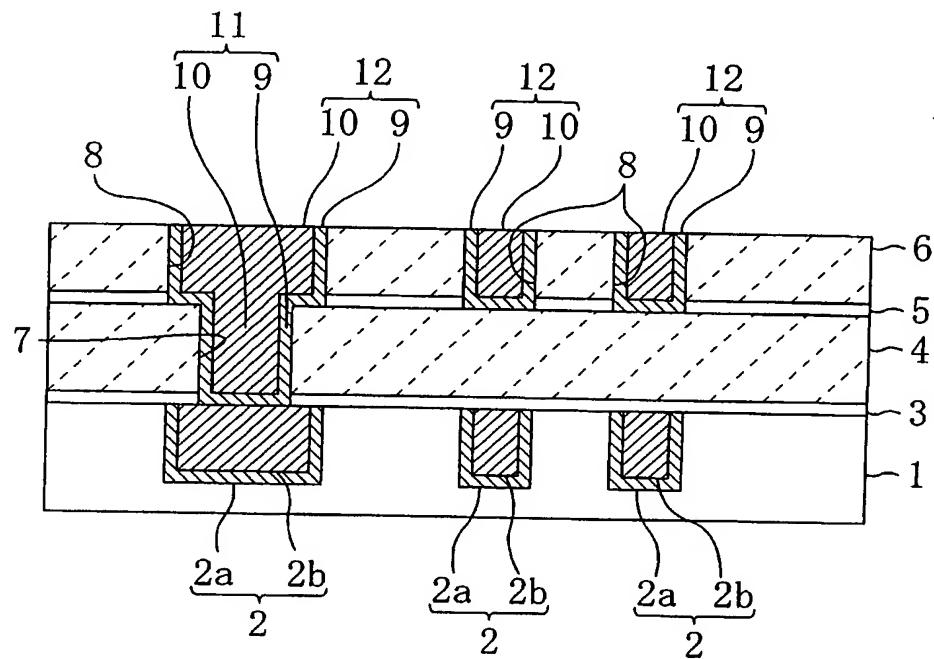
【図5】 [FIG.5]



【図6】 [FIG. 6]



【図7】 [FIG. 7]



【図8】 [FIG. 8]

